Register No : _____

THE KAVERY ENGINEERING COLLEGE

(An Autonomous Institution)

B.E/B.TECH DEGREE END SEMESTER THEORY EXAMINATIONS, NOV/DEC 2025

Third Semester

Electrical and Electronics Engineering

UEET24301- Digital Logic Circuits

Regulations - 2024

Duration : 3 Hrs *Maximum : 100 Marks*

*PART – A (ANSWER ALL QUESTIONS) (Marks 10*2=20)*

Q.No	*Questions*	*BTL*	*CO*	*Marks*
1.	Define number system and list different types.	L1	1	2
2.	State De-Morgan's theorems.	L1	1	2
3.	Draw the block diagram of a 3-to-8 decoder.	L1	2	2
4.	compare between half adder and full adder.	L2	2	2
5.	Draw the truth table of SR flip-flop.	L1	3	2
6.	Define synchronous sequential circuit.	L1	3	2
7.	List the types of hazards in asynchronous sequential circuits.	L1	4	2
8.	Write the advantages of using PLDs over fixed logic implementation.	L1	4	2
9.	Outline the need for Test bench.	L2	5	2
10.	Classify the different types of test bench.	L2	5	2

*PART – B (ANSWER ALL QUESTIONS) (Marks 5*16 = 80)*

Q.No		*Questions*	*BLT*	*CO*	*Marks*
11.	a	A communication system requires minimum hardware design. Simplify the function using K-map to reduce hardware: F (A, B, C, D) =Σm (1,3,4,5,7,11,15). Implement with logic gates.	L3	1	16
		Or			
	b	Convert the following numbers into the indicated bases: (i) (1011101)2 to decimal (ii) (356)8 to binary (iii) (A3)16 to binary (iv) $(275)_{10}$ to hexadecimal	L3	1	16
12.	a	Analyze the working of an 8-to-3 encoder with truth table and logic diagram.	L4	2	16
		Or			
	b	Simplify a half subtractor and full subtractor with suitable logic diagrams.	L4	2	16

13.	a		Determine the a 4-bit synchronous up/down counter using T flip-flops. Show excitation table, logic diagram, and timing diagram.	L5	3	16
			Or			
	b	i	Explain the operation, state diagram and characteristics of a T-Flip flop.	L5	3	8
		ii	Evaluate the design procedure with neat diagram about 4-bit bidirectional shift register with parallel load.	L5	3	8
14.	a		Build about the following programmable logic devices: (i) PLA (ii) PAL	L3	4	16
			Or			
	b		Organize an asynchronous sequential circuit with two inputs x1 and x2 and one output Z. Initially, both inputs are equal to zero. When x1 or x2 becomes 1, the output Z becomes 1. When the second input also becomes 1, the output changes to 0. The output stays at 0 until the circuit goes back to the initial state.	L3	4	16
15.	a		Assess in detail the design procedure for register transfer language.	L5	5	16
			Or			
	b		Compare the VHDL code for full subtractor in structural modeling and data flow modeling.	L5	5	16